CLAIMS:

WHAT IS CLAIMED IS:

1. A method for estimating a phase error comprising:

inputting a first signal component spread by a first spreading code and an orthogonal second signal component spread by a second spreading code;

determining a cross-despread value by despreading the first signal component with the second spreading code;

calculating an estimate of interference from the second signal component into the first signal component; and

estimating a phase error by canceling the estimate of interference from the cross-despread value.

2. The method of claim 1 wherein calculating an estimate of interference comprises

determining an estimate of a data symbol of the first signal component by despreading the first signal component with the first spreading code, and

multiplying the estimate of the data symbol of the first signal component by the first and second spreading codes.

3. The method of claim 2 wherein calculating an estimate of interference further comprises summing, over all chips per symbol for the second spreading code, the products of the estimates of the data symbols of the first signal component multiplied by the first and second spreading codes.

4. The method of claim 1 wherein the cross-despread value is a first cross-despread value and the estimate of interference is a first estimate of interference, the method further comprising:

determining a second cross-despread value by despreading the second signal component with the first spreading code;

calculating a second estimate of interference from the first signal component into the second signal component; and

estimating a phase error comprises calculating IdQ_C by canceling the first estimate of interference from the first cross-despread value, calculating QdI_C by canceling the second estimate of interference from the second cross-despread value, and outputting an estimate of phase error based on at least one of IdQ_C and QdI_C.

5. The method of claim 4 wherein outputting an estimate of phase error based on at least one of IdQ_C and QdI_C comprises driving each of IdQ_C and QdI_C to a common rate IdQ_A and QdI_A, respectively, and summing the results to obtain the estimate of phase error.

6. The method of claim 5 wherein driving each of IdQ_C and QdI_C to a common rate comprises summing, over a multiple of chips per symbol that is common to both the first signal component and the second signal component.

7. The method of claim 5 wherein outputting an estimate of phase error further comprises, prior to summing the results:

scaling IdQ_A with a scaling factor derived from the second signal component; and

scaling QdI_A with a scaling factor derived from the first signal component..

8. The method of claim 7 wherein each of the scaling factors λ_I and λ_Q are selected to maximize a signal to noise ratio in the estimate of phase error.

9. A phase error detector comprising:

a first input for receiving a first signal component spread with a first component spreading code;

a first despreader having an input coupled to the first input for despreading the first signal component with a second component spreading code associated with a second signal component that is orthogonal to the first;

a second despreader having an input coupled to the first input for depsreading the first signal component with the first component spreading code;

a first discriminator having an input coupled to an output of the second despreader for outputting a data symbol estimate of the first signal component;

a first multiplier having an input coupled to the first discriminator for multiplying the data symbol estimate of the first signal component by the first and second component spreading codes; and

a first adder having inputs coupled to an output of the multiplier and to an output of the first despreader.

10. The phase error detector of claim 9 further comprising:

a second multiplier having an input coupled to an output of the first adder for multiplying said input by a scaling factor.

11. The phase error detector of claim 9 further comprising a first summing block disposed between the first discriminator and the first adder, said summing block for summing, over all chips per symbol of the second spreading code, the products of the first and second spreading codes.

12. The phase error detector of claim 9 further comprising:

a second input for receiving a second signal component that is orthogonal to the first signal component, the second signal component spread with the second component spreading code;

a third despreader for despreading the second signal component with the first component spreading code;

a fourth despreader in parallel with the third for depsreading the second signal component with the second component spreading code;

a second discriminator having an input coupled to an output of the fourth despreader for outputting a data symbol estimate of the second signal component;

a third multiplier having an input coupled to the second discriminator for multiplying the data symbol estimate of the second signal component by the first and second component spreading codes; and

a second adder having inputs coupled to an output of the third multiplier and to an output of the third despreader.

13. The phase error detector of claim 12 further comprising:

a second multiplier having inputs coupled to an output of the first adder and to a first scaling factor;

a fourth multiplier having inputs coupled to an output of the second adder and to a second scaling factor; and

a third adder having inputs coupled to outputs of the second and fourth multiplier, and an output coupled to a feedback loop.

14. The phase error detector of claim 12 further comprising a second summing block disposed between the second discriminator and the second adder, said second summing block for summing, over all chips per symbol of the first signal component, the products of the first and second spreading codes.

15. The phase error detector of claim 14 further comprising:

a third summing block having an input coupled to an output of the first adder; and

a fourth summing block having an input coupled to an output of the second adder,

wherein said third and fourth summing blocks operate to provide outputs at a common symbol rate.

16. The phase error detector of claim 15 further comprising

a fifth multiplier having inputs coupled to an output of the first adder and to an output of the second discriminator, said fifth multiplier having an output coupled to the input of the third summing block; and

a sixth multiplier having inputs coupled to an output of the second adder and to an output of the first discriminator, said fifth multiplier having an output coupled to the input of the fourth summing block.

17. In a phase error detector defining a first input for receiving a first signal component spread with a first spreading code, the improvement comprising:

a first despreader for despreading the first signal component with a second spreading code;

means for determining a first interference term from despreading the first signal component with the second spreading code;

a first combiner for removing said first interference term from said first signal component despread with said second spreading code.

18. In the phase error detector of claim 17 wherein the phase error detector further comprises a second input for receiving a second signal component orthogonal to the first signal component, said second signal component spread with the second spreading code, the improvement further comprising:

a second despreader for despreading the second signal component with the first spreading code;

means for determining a second interference term from despreading the second signal component with the first spreading code;

a second combiner for removing said second interference term from said second signal component despread with the first spreading code.

19. In the phase error detector of claim 18, the improvement further comprising:

a first multiplier for applying a symbol estimate derived from the second signal component to an output of the first combiner;

a first summing block for converting an output of the first multiplier to a common rate;

a second multiplier for applying a symbol estimate derived from the first signal component to an output of the second combiner; and

a second summing block for converting an output of the second multiplier to the common rate.

20. The phase error detector of claim 19, the improvement further comprising:

a third multiplier for applying a first scaling factor derived from the second signal component to an output of the first summing block;

a fourth multiplier for applying a second scaling factor derived from the first signal component to an output of the second summing block; and

a third combiner for combining scaled outputs of said third and fourth multipliers.